# EDA Tool Compatibility

* Cadence EDA tools were used for verification and synthesis of this product.
* Xcelium 19.03-s003
* Design Compiler RTL Synthesis N-2017.09-SP3
* HAL Linting tool 15.20.027
* Conformal 16.20.s240
* Compatibility testing has been done with VCS N-2017.12-SP2-4.
* For Platform Architrect, used GCC version is gcc-6.1.0a. (Backward compatible upto gcc-5.2.0-64)
* Please refer to IP Integration specification to enable/disable specific CFG checker in order to resolve or workaround any verification related issues, if any.

Contact your CFG or Synopsys support team for assistance.